ABSTRACT OF THE DISCLOSURE

A sampling clock generator circuit comprises a ring oscillator including series-connected m first inverters connected to a first power supply line, where m is an odd number equal to or larger than 3, a delay line including series-connected 2m or 2m-1 second inverters connected to a second power supply line, for delaying an externally supplied clock, and a PLL circuit for controlling an oscillation frequency of the ring oscillator by controlling a voltage of the first power supply line by using the ring oscillator as a voltage controlled oscillation circuit. A voltage of the second power supply line is set substantially equal to the voltage of the first power supply line and the delayed clock obtained by the second inverters is used as a sampling clock.